PHD/PHP36N03LT

N-channel TrenchMOS logic level FET

Rev. 02 — 8 June 2006 **Product data sheet**

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Logic level compatible
- Low gate charge

1.3 Applications

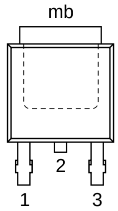
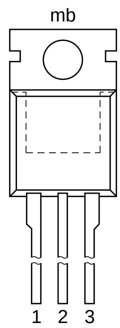
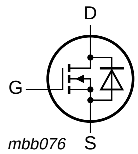
- DC-to-DC converters
- Switched-mode power supplies

1.4 Quick reference data

- $V_{DS} \leq 30$ V
- $I_D \leq 43.4$ A
- $R_{DSon} \leq 17$ mΩ
- $P_{tot} \leq 57.6$ W

2. Pinning information

Table 1. Pinning

Pin	Description	Simplified outline		Symbol
1	gate (G)			
2	drain (D) [1]			
3	source (S)			
mb	mounting base; connected to drain			
		SOT428 (DPAK)	**SOT78 (3-lead TO-220AB)**	

[1] It is not possible to make a connection to pin 2 of the SOT428 package.

3. Ordering information

Table 2. Ordering information

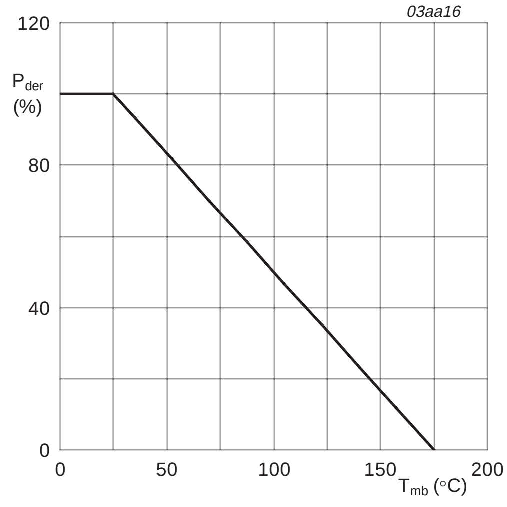
Type number	Package		
	Name	Description	Version
PHD36N03LT	DPAK	plastic single-ended surface-mounted package; 3 leads (one lead cropped)	SOT428
PHP36N03LT	SC-46	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

4. Limiting values

Table 3. Limiting values

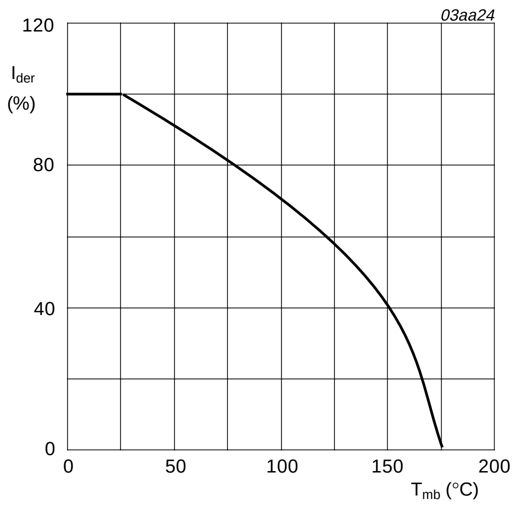
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C	-	30	V
V_{DGR}	drain-gate voltage (DC)	25 °C ≤ T_j ≤ 175 °C; R_{GS} = 20 kΩ	-	30	V
V_{GS}	gate-source voltage		-	±20	V
I_D	drain current	T_{mb} = 25 °C; V_{GS} = 10 V; see Figure 2 and 3	-	43.4	A
		T_{mb} = 100 °C; V_{GS} = 10 V; see Figure 2	-	30.7	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs; see Figure 3	-	173.6	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; see Figure 1	-	57.6	W
T_{stg}	storage temperature		–55	+175	°C
T_j	junction temperature		–55	+175	°C
Source-drain diode					
I_S	source current	T_{mb} = 25 °C	-	43.4	A
I_{SM}	peak source current	T_{mb} = 25 °C; pulsed; t_p ≤ 10 µs	-	173.6	A



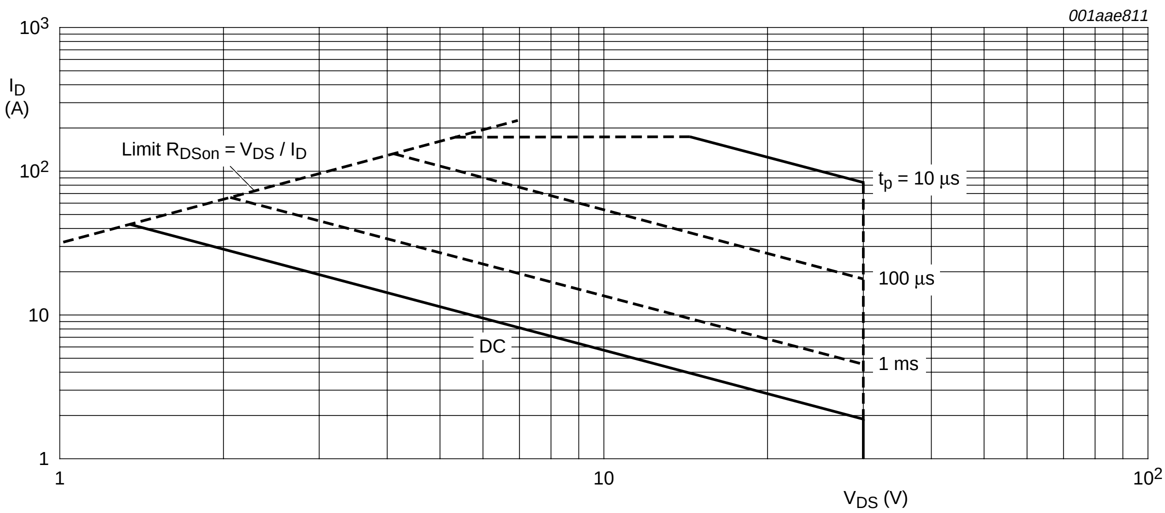
$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature



$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse; V_{GS} = 10 V

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4		-	-	2.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient						
	SOT78	vertical in free air		-	60	-	K/W
	SOT428	minimum footprint	[1]	-	75	-	K/W
		SOT404 minimum footprint	[1]	-	50	-	K/W

[1] Mounted on a printed-circuit board; vertical in still air.

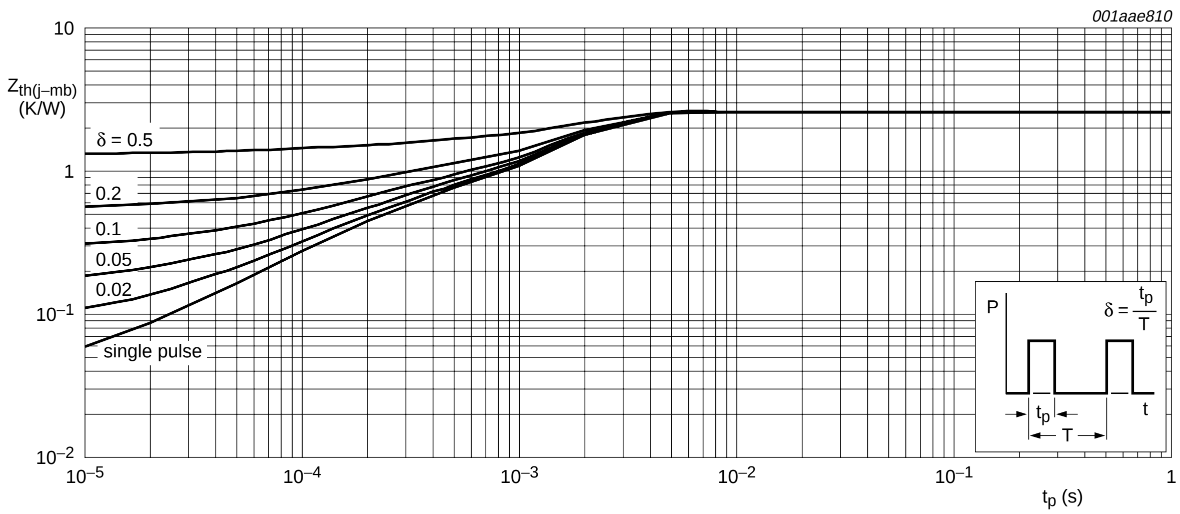


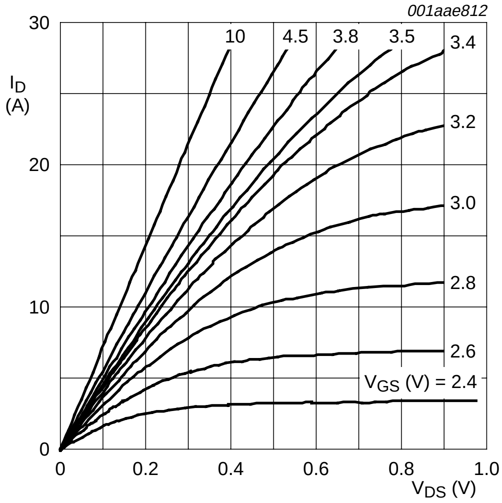
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

6. Characteristics

Table 5. Characteristics

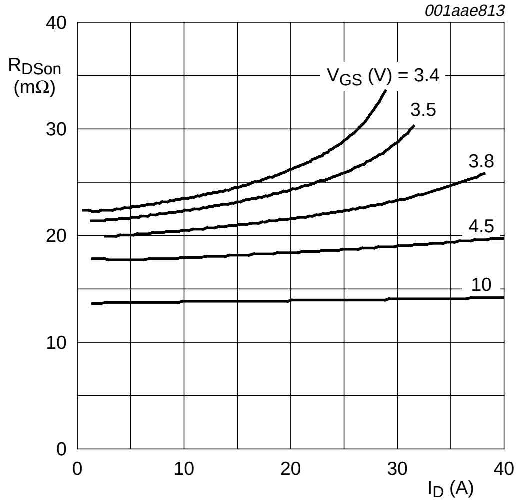
T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 μA; V_{GS} = 0 V				
		T_j = 25 °C	30	-	-	V
		T_j = –55 °C	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 250 μA; V_{DS} = V_{GS}; see Figure 9 and 10				
		T_j = 25 °C	1	1.5	2	V
		T_j = 175 °C	0.5	-	-	V
		T_j = –55 °C	-	-	2.2	V
I_{DSS}	drain leakage current	V_{DS} = 24 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	1	μA
		T_j = 175 °C	-	-	500	μA
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 12 A; see Figure 6 and 8				
		T_j = 25 °C	-	18	22	mΩ
		T_j = 175 °C	-	32.4	39.6	mΩ
		V_{GS} = 10 V; I_D = 25 A; see Figure 6 and 8	-	14	17	mΩ
		V_{GS} = 3.5 V; I_D = 5.2 A; see Figure 6 and 8	-	22	40	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 36 A; V_{DS} = 15 V; V_{GS} = 10 V; see Figure 11 and 12	-	18.5	-	nC
Q_{GS}	gate-source charge		-	4.2	-	nC
Q_{GD}	gate-drain charge		-	2.9	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; see Figure 14	-	690	-	pF
C_{oss}	output capacitance		-	160	-	pF
C_{rss}	reverse transfer capacitance		-	110	-	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 15 V; R_L = 0.6 Ω; V_{GS} = 10 V; R_G = 10 Ω	-	6	-	ns
t_r	rise time		-	10	-	ns
$t_{d(off)}$	turn-off delay time		-	33	-	ns
t_f	fall time		-	19	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; see Figure 13	-	0.97	1.2	V



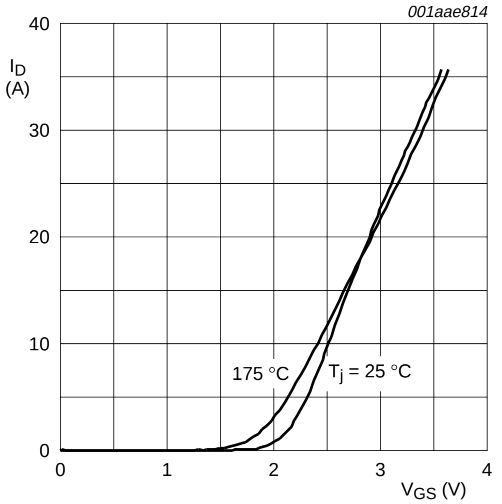
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values



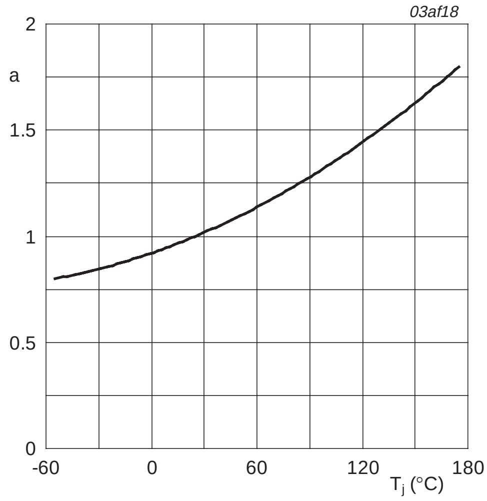
T_j = 25 °C

Fig 6. Drain-source on-state resistance as a function of drain current; typical values



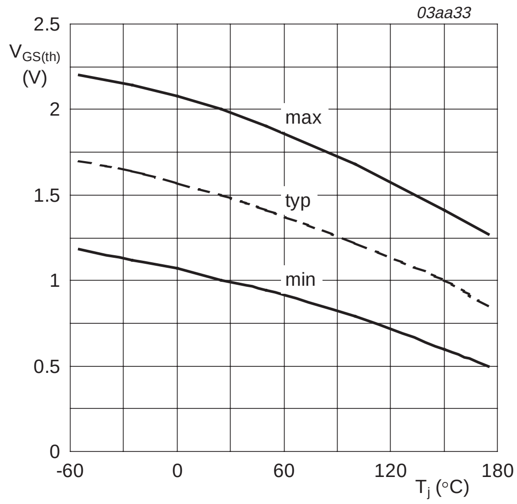
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values



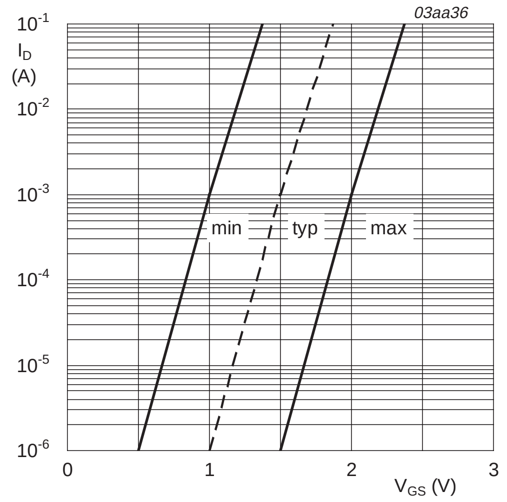
$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature



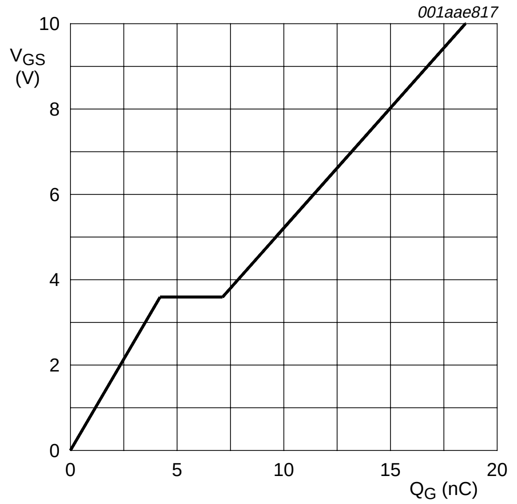
I_D = 1 mA; $V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature



T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage



I_D = 36 A; V_{DS} = 15 V

Fig 11. Gate-source voltage as a function of gate charge; typical values

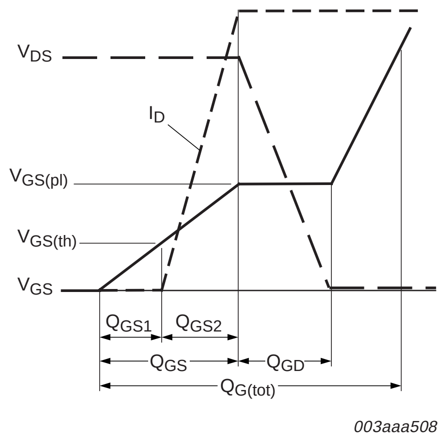
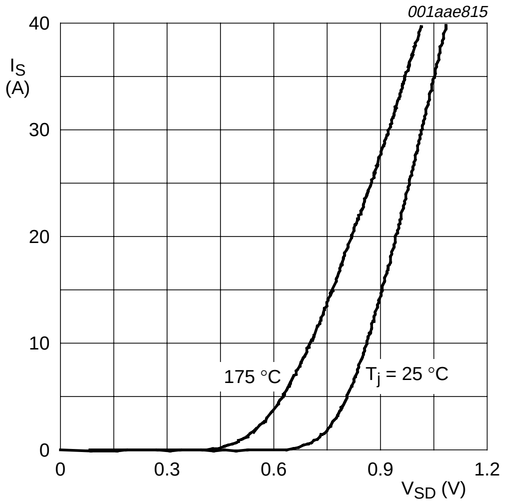
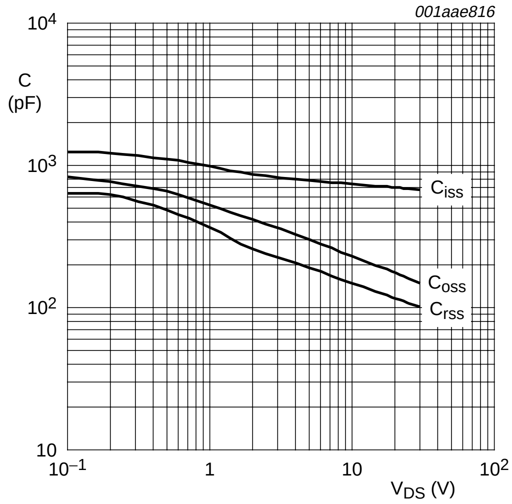


Fig 12. Gate charge waveform definitions



T_j = 25 °C and 175 °C; V_{GS} = 0 V

Fig 13. Source current as a function of source-drain voltage; typical values

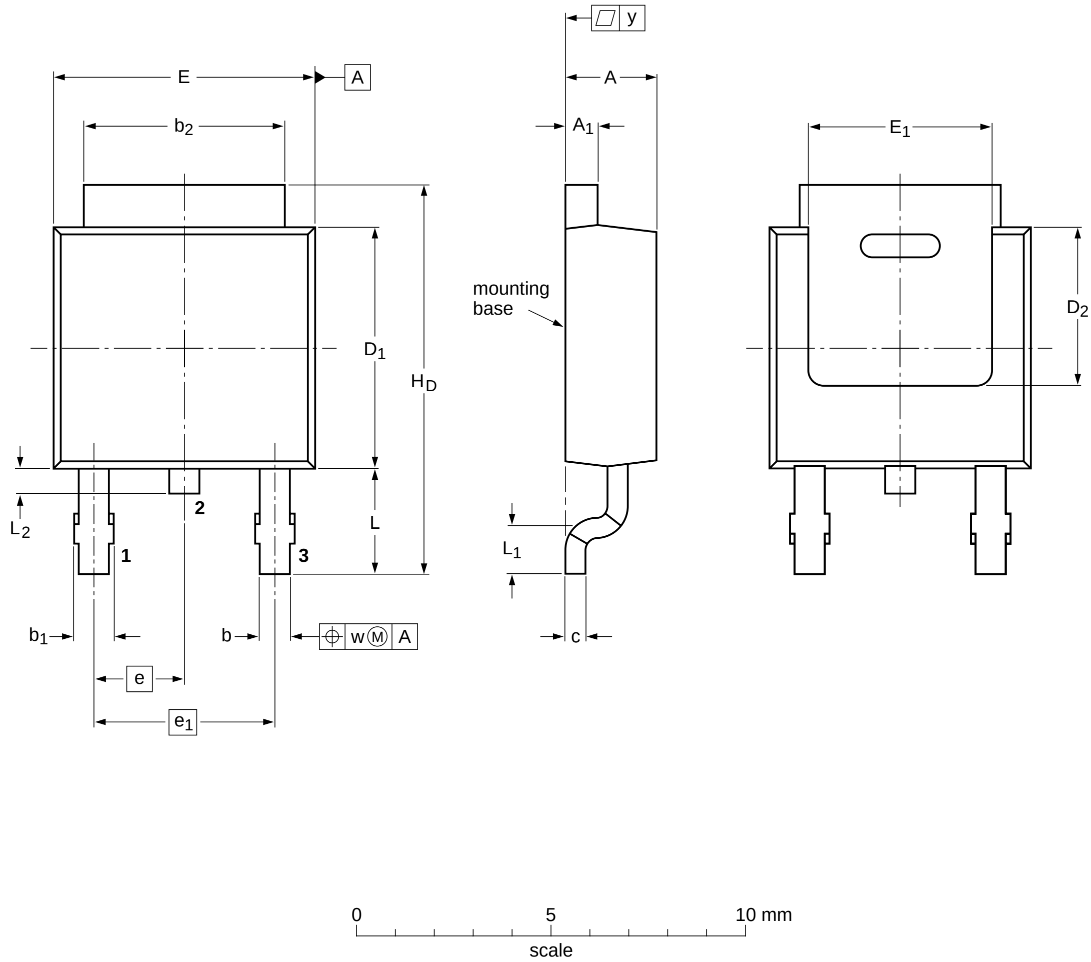


V_{GS} = 0 V; f = 1 MHz

Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D_1	D_2 min	E	E_1 min	e	e_1	H_D	L	L_1 min	L_2	w	y max
mm	2.38 2.22	0.93 0.46	0.89 0.71	1.1 0.9	5.46 5.00	0.56 0.20	6.22 5.98	4.0	6.73 6.47	4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

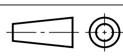
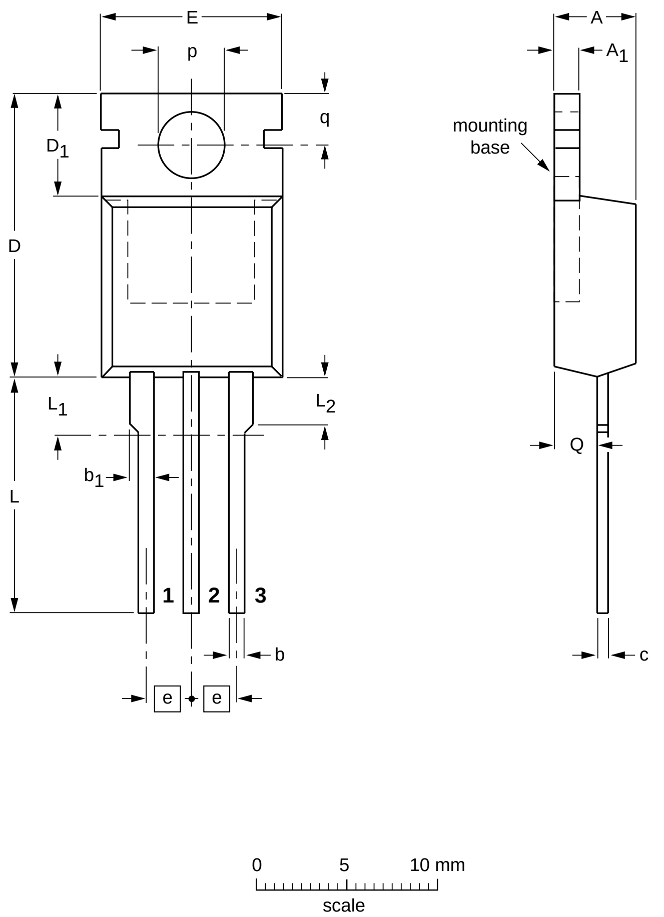
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~06-02-14~~ 06-03-16

Fig 15. Package outline SOT428 (DPAK)

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	L_2 max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.45 1.00	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~05-03-22~~ 05-10-25

Fig 16. Package outline SOT78 (3-lead TO-220AB)

8. Revision history

Table 6. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHD_PHP36N03LT_2	20060608	Product data sheet	-	PHD36N03LT-01
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Addition of PHP36N03LT			
PHD36N03LT-01 (9397 750 11613)	20030630	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.semiconductors.philips.com.

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11. Contents

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